ISSN:0975-9646
Rajendra Prasad S et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 2 (6) , 2011, 2761-2764

A New Low Power 9T SRAM Cell based on CNTFET at 32nm Technology Node

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***Abstarct*---- This paper proposes a new design of highly stable and low power SRAM cell using carbon nanotube FETs (CNTFETs) at 32nm technology node. As device physical gate length is reduced to below 65 nm, device non-idealities such as large parameter variations and exponential increase in leakage current make the I-V characteristics substantially different from traditional MOSFETs and become a serious obstacle to scale devices. CNFETs have received widespread attention as one of the promising successor to MOSFETs. The proposed circuit was simulated in HSPICE using 32nm Stanford CNFET model. Analysis of the results shows that the proposed CNTFET based 9T SRAM cell, power dissipation, and stability substantially improved compared with the conventional CMOS 6T SRAM cell by 51% and 58% respectively at the expense of 4% write delay increase.**

***Keywords*----- SRAM, CNTFET, CMOS, low power, highly stable**

I. INTRODUCTION

For the foreseeable feature, static random access memory (SRAM) will likely remain as the embedded memory technology of choice for many microprocessors and systems on chips (SoCs) due to the speed advantage and compatibility with standard logic processes. With the advent of SoC, the design of highly stable and power efficient SRAM structures has become highly desirable. Therefore, it is essential to develop a low power SRAM design technique for the new device technology such as CNTFET.

Carbon Nanotube Field Effect Transistor (CNFET) is the most promising technology to extend or complement the traditional silicon technology due to the following three reasons: First, the operation principle and the device structure are similar to CMOS devices, and the established CMOS design infrastructure can be utilized. Second, the CMOS fabrication process can still be utilized. And the most important reason is that CNFET has the best experimentally demonstrated device current carrying capability so far. Several researches have been done to estimate the performance of CNFET at a single device level in the presence of process related non-idealities and imperfections at the 32 nm technology node using compact CNFET SPICE model [1][2].

In this paper, as a circuit level design of CNTFET, a novel low power and highly stable 9T SRAM cell design is proposed and its performance and viability are demonstrated by performing various simulations. The stability and power consumption of the 9T SRAM cell based on CNTFET are compared with that of the conventional CMOS 6T SRAM cell design to show the viability of the CNTFET based SRAM cell design.

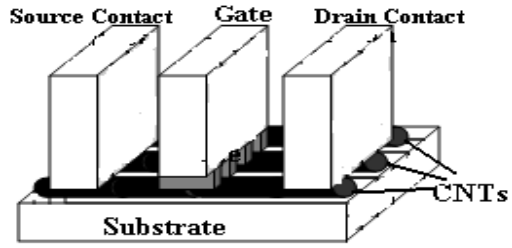
The circuit simulation in this paper uses a 32nm CNFET HSPICE model that includes the practical device non-idealities for CNFET [3][4] and the 32nm BSIM PTM (predictive technology model) for Si MOSFET [5].

This paper is organized in the following manner: The characteristics and physical features of CNTFET Transistor are explained in section II, and section III describes, the mechanisms of the read and write operations of the proposed 9T CNTFET SRAM cell and the schemes for deciding the number of nanotubes of each. The simulation results are presented in section IV to compare the performance and viability of the CNTFET technology with that CMOS technology, and followed by the conclusion in Section V.

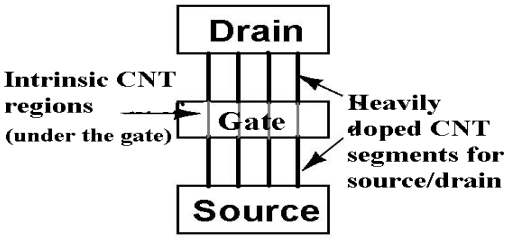
II. CNTFET TRANSISTOR

Carbon nanotube Field Effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electronic devices; CNTFETs have been shown to have similar properties to MOSFETs. A single-wall carbon nanotube (or SWCNT) consists of only one cylinder, and the simple manufacturing process of this device makes it a very promising alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m) [6]. A simple method to determine if a carbon nanotube is metallic or semiconducting is based on considering the indices (n, m), i.e. the nanotube is metallic if $n=m$ or $n-m=3i$ where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated from [6] as a function of m and n. Fig. 1 shows the schematic diagram of the CNTFET [6]. Similar to the silicon device the CNTFET has four terminals, a dielectric film is wrapped around a portion of the undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Fig. 2 shows the equivalent circuit model implemented in HSPICE as proposed in [6]. Heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance during the on-state [7]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

The current-voltage (I-V) characteristics of the CNTFET are shown in Fig. 3, and they are similar to those of MOSFET. The CNTFET device current is saturated at higher Vds (drain to source voltage) as channel length increases as shown in Fig. 3, and the on-current decreases due to energy optimization in the axial direction at 32-nm (or less) gate length [6].



(a)



(b)

Fig. 1 Schematic diagram of a carbon nanotube transistor (CNTFET):
(a) sectional view; (b) top view

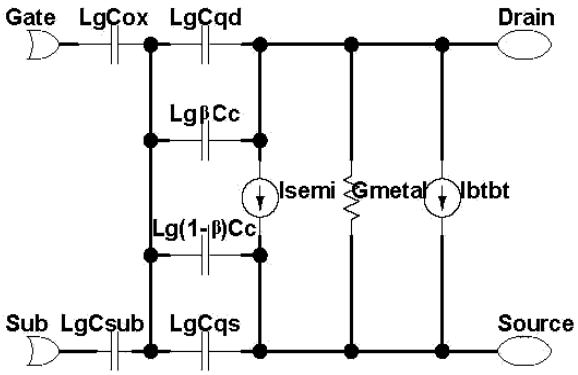


Fig. 2 Equivalent circuit model for the intrinsic channel region of a CNTFET [6]

III.PROPOSED 9T CNTFET SRAM CELL

A new 9T CNTFET SRAM cell structure is proposed in this paper to increase SNM and to reduce the power consumption of the SRAM cell.

A. Write and Read Operations

The write and read bits are separated in this new 9T CNTFET SRAM cell. While in traditional 6T CMOS SRAM both bit and bit-bar lines are used for writing data, but in this newly proposed 9T CNTFET SRAM cell only Write_Bit is used to write both "0" and "1" data, as shown in fig. 4. The writing operation starts by disconnecting the feedback loop of the two inverters. By setting 'W_bar' signal to "0", the feedback loop is disconnected. The data that is going to be written is determined by the Write_Bit voltage. If the feedback connection is disconnected, SRAM cell has just two back-to-back connected inverters. Write_Bit transfers the complementary of the input data to Q2, which drives the other inverter (M1 and M2) to develop Q_bar. Write_Bit have to be pre-charged "high" before and right after each write operation. When writing "0" data at Q2, negligible writing power is consumed because there is no discharging activity at Write_Bit. To write '1' data at Q2, the Write_Bit have to be discharged to ground level just like 6T CMOS SRAM cell. In this case, the dynamic power consumed by the discharging is the same as 6T CMOS SRAM. The write circuit does not discharge for every write operation but discharges only when the cell writes "1" data, and the activity factor of the discharging Write_Bit is less than "1", which makes the proposed 9T CNTFET SRAM cell more power effective during writing operation compared with the conventional CMOS SRAM cell.

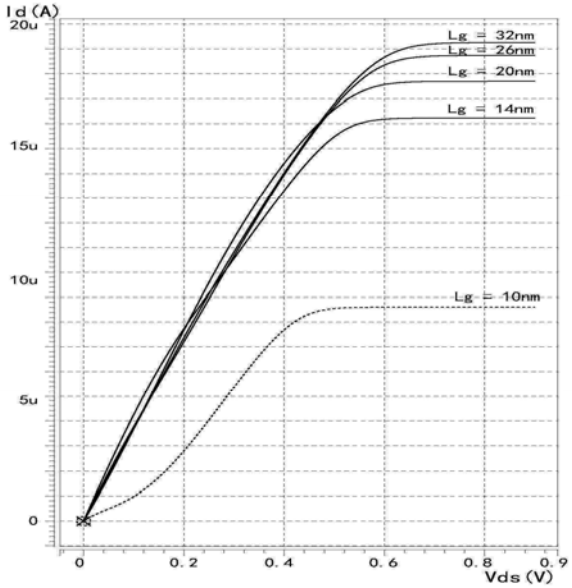


Fig. 3 Current-voltage (I-V) characteristics of a ballistic CNTFET

The first step in the read operation is the pre-charging of all the Read_Bit lines. During read operation, transistor M7 is turned on by setting W_bar signal high and the Read_Row (RD) "high" to turn on M8 and M9. When Q2="0", the M6 is turned off making the Read_Bit voltage not change from the pre-charged value, which means the cell data Q2 holds "0". On the other hand, if Q2 is "1", the transistors M6, M8 and M9 are turned on. In this case, due to charge sharing, the Read_Bit voltage will be dropped about 100~ 200mV and this voltage drop is enough to be detected in the sense amplifier.

B. CNTFET configuration

When writing "0", Write_Bit is pre-charged high (V_{DD}) and M7 is turned off. The node voltage at Q1 is less than V_{DD} due to the threshold voltage drop between the gate and source of the transistor M5. To compensate this voltage drop, the transistor M3 and M4 must be designed as a low-skew inverter to guarantee that Q2 is at a solid ground level to represent "0" state. A low-skewed inverter has a weaker PMOS transistor. If the PMOS CNTFET has only one tube, the current can be minimized. On the other hand, the operation of writing "1" is stable because NMOS transistor M5 can pass "0" faithfully.

Assume that initially the cell stores "0" at Q2 and "1" at Q_bar after WL (Word Line) is deactivated and W_bar is activated. In this case, the voltage at Q1 is less than V_{DD} due to the threshold voltage drop across the gate and source of the transistor M7. The degraded voltage at Q1 may turn on the transistor M4 slightly causing short circuit current through transistors M4 and M3. To overcome this problem, the low skewed inverter (M3 and M4) mentioned

for writing "0" case is justified again and the V_{th} of the transistor M7 needs to be controlled low to reduce the voltage difference between Q_bar and Q1.

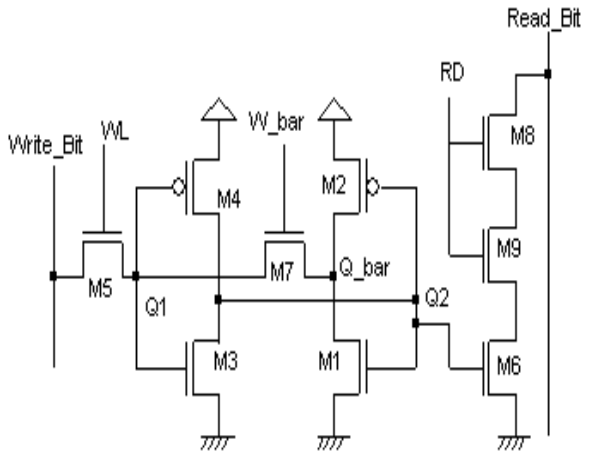


Fig. 4 The proposed 9T CNTFET SRAM Cell structure

Transistor ratio of M3 to M4 should be at least 2, to implement a low skewed inverter with transistors M3 and M4, to have a solid ground level at Q2. However, by increasing the number of tubes, the M4 and M3 area sizes can be same. That is, if M4 has only one tube and M3 has 2 tubes, then the current ratio M3/M4 can be more than 2. This means that the inverter transistor sizes M3/M4 can be smaller than 2 by controlling the number of tubes. Transistor ratio M5/M4 of 1.3, M1/M4 of 3, and low V_{th} of the transistor M7 guarantees a stable READ operation when Q_bar stores "0". However, if the similar approach to M3/M4 sizing is used to optimize transistor ratios among M1, M5 and M4, the transistor sizes can be further reduced. If M5 has only one tube, M1 has two tubes and M4 has one tube, the transistor M1 needs to be only 1.5 times larger than transistor M4 to satisfy the relationships among M1, M5, and M4.

By utilizing the CNTFETs threshold voltage controllability and transistor sizing techniques, the newly proposed 9T CNTFET SRAM cell can accomplish low power consumption due to tuning V_{th} and the smaller node capacitance, at the minimal cost of the area overhead.

IV. SIMULATION RESULTS

6T SRAM and 9T SRAM cells are designed using bulk CMOS and CNTFET transistors respectively. HSPICE simulations are performed at 32nm technology node using the Stanford CNTFET model and the Predictive Technology Model **(**PTM) to compare the performance of the 9T CNTFET and 6T CMOS SRAM cells.

A. Simulation Setup

The following technology parameters are used for simulation of 9T SRAM cell using CNTFET Technology: Lch (physical channel length) = 32.0nm, Lss (the length of the doped CNT drain-side/source-side extension region) = 32.0nm, Efi (Fermi level of the doped S/D tube) = 0.6 eV, Tox (The thickness of high-k top gate dielectric material) = 4.0nm, (n1, n2) (chirality of tube) = (19,0), pitch = 10nm, V_{fbn} and V_{fbp} (Flatband voltage for n-CNTFET and p-CNTFET) = 0.0eV and 0.0eV, physical gate length = 32.0nm, Lgeff (the mean free path in intrinsic CNT channel region due to non-ideal elastic scattering) = 200.0nm, Lss/Ldd (the length of the doped CNT source/drain extension region) = 32.0nm, the mean free path in p+/n+ doped CNT = 15.0nm, the work function of Source/Drain metal contact = 4.6eV, and CNT work function = 4.5eV.

The minimum transistor sizes used for CMOS and CNTFET technologies are W=48nm and L = 32nm for bulk CMOS, and L=32nm and the number of tubes =1 for CNTFET. A Power supply of 0.9 V is used [8]. Table 1 shows the summarized results to compare the proposed 9T CNTFET SRAM characteristics with the conventional CMOS 6T SRAM cell.

B. Dynamic Power Consumption

The newly proposed 9T CNTFET SRAM cell achieves 51% writing power saving while maintaining the cell performance, read/write delay, and stability of the conventional cell. The power saving comes from the fact that the cell keeps Write_Bit "high" instead of discharging when it writes "0", which reduces the activity factor of the Write_Bit.

TABLE I
SUMMARIZED SIMULATION RESULTS

	6T CMOS SRAM	**9T CNTFET SRAM**
Dynamic Power (W)	1.98E-06	9.702E-07
Leakage Power (nW)	112	108.64
Write Delay (pS)	34.2	35.568
Read Delay (pS)	24.87	23.37
SNM (mV)	122	192.76

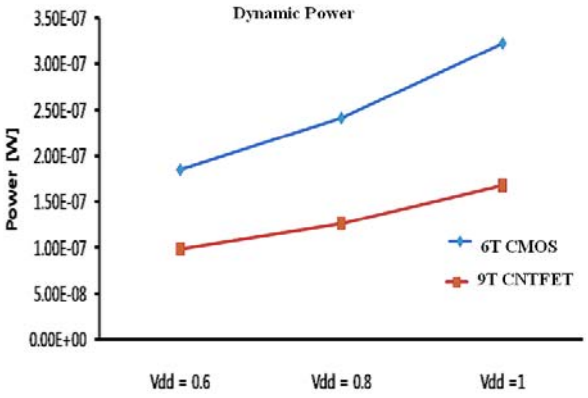


Fig. 5 The Dynamic Power Consumption with V_{DD} variation

While conventional 6T CMOS SRAM always discharges one of the bit lines to write a data into the cell, the proposed 9T CNTFET SRAM discharges the Write_Bit only when it writes "1". As the probability of writing '0' gets higher, the power dissipation due to the bit line discharging is reduced comparing to the conventional case. Fig. 5 shows the dynamic power consumption of the CNTFET 9T SRAM cell for different V_{DD}. As shown in the Fig. 5, the power saving of the 9T CNTFET SRAM cell becomes greater as V_{DD} increases since the dynamic power difference between the 6T CMOS SRAM and the proposed 9T CNTFET SRAM cell increases exponentially as V_{DD} increases.

C. Leakage Power Consumption

Fig. 6 and Table I shows the leakage power of the 6T CMOS SRAM cell and 9T CNTFET SRAM cell. In the

9T CNTFET SRAM cell, the bitline leakage is significantly reduced by adding a NMOS transistor (M9), because of the so-called "stack effect" between M8 and M9. The reduced bitline leakage makes it possible to have more SRAM cells on a bitline for high-density SRAM designs.

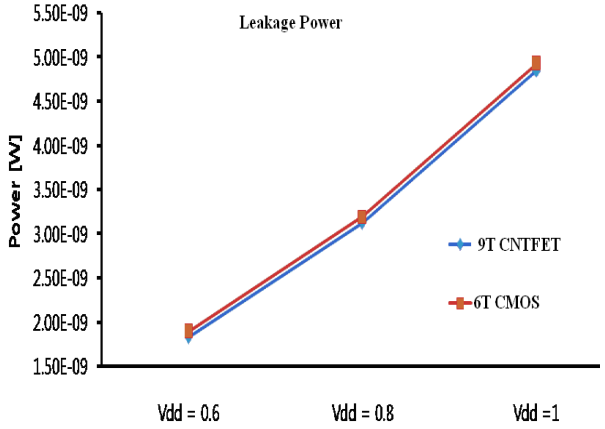


Fig. 6 The Dynamic Power Consumption with V_{DD} variation

As a result, the leakage current through the Read_Bit, M6, M8 and M9 path is relatively small. The leakage current in 9T CNTFET SRAM is less than 3% compared to 6T CMOS SRAM.

D. Static Noise Margin

Static Noise Margin (SNM) is the standard metric to measure the stability in SRAM bit-cells. The SNM of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. The voltage transfer curves (VTCs) of the back-to-back inverters in a bit-cell are used to measure SNM. Separating the Read and Write bit offers wider SNM during read operation as shown in Fig. 7. When reading the stored data, only Read_Bit affects inverter1 (M1/M2) output voltage. Consequently, this fact makes the cell hard to flip. Table 1 shows 9T CNTFET SRAM cell has the highest SNM because of the relatively higher V_{th} and lower leakage current than CMOS based SRAM cells.

E. Write and Read Delay

For write operation, the write delay is defined as the time from the 50% activation of the WL to the time when Q_bar becomes 90% of its full swing. The write delay is approximately equal to the propagation delay of the inverter2 (M3/M4) and inverter1 (M1/M2). Because the inverter1 is only driving the diffusion capacitor of M7, it is desirable to reduce the input capacitance of the inverter1 as much as possible to reduce the load capacitance on inverter2. The proposed 9T CNTFET SRAM cell is slightly slower than 6T SRAM in writing operation because of this reason.

The read time depends on the READ path's transistors' sizes. The proposed 9T CNTFET SRAM cell READ delay is almost same as the conventional 6T CMOS SRAM cell since the transistor sizes are very similar. The READ access time at the cell level is determined by the time taken for the bitlines to develop a potential difference of at least 100mV.

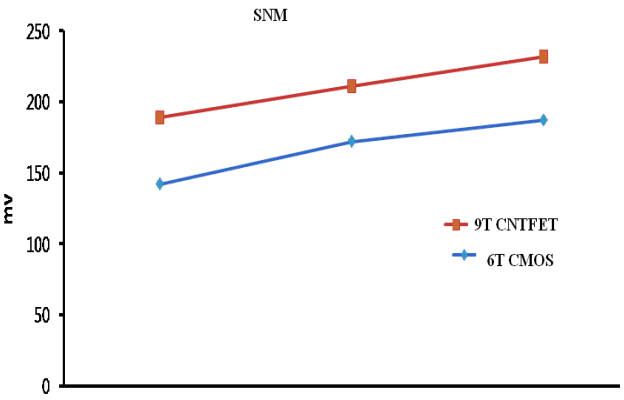


Fig. 7 SNM for 6T and proposed 9T CNTFET cell with V_{DD} Variation

V. CONCLUSION

This paper has investigated the use of MOSFET-like CNTFET in place of the conventional CMOS in the design of SRAM cell. This new 9T CNTFET SRAM cell is compared with CMOS based 6T SRAM cell. This new 9T CNTFET SRAM cell cuts off the feedback connection between the two back-to-back inverters in the SRAM cell when data is written and separates the write and read port with 9 transistors. Compared to 6T SRAM structure, the proposed 9T CNTFET SRAM saves power up to 51% and obtains 58% higher SNM during read operation at the minimal cost of 4% delay increase. These Simulation results show that the CNTFET based 9T SRAM cell design achieves improvements in stability and power consumption, especially at a low power supply.

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